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**IN THE CLAIMS:**

Please amend the claims as follows:

1. (Currently Amended) A semiconductor device assembly comprising:  
a substrate having a surface, having a passivation layer provided over at least a portion of said surface of said substrate, having a second passivation layer provided over at least a portion of said first passivation layer, having a layer comprising substantially diamond provided over at least a portion of said ~~surface of said substrate~~ second passivation layer having at least one aperture therein, and having at least one contact pad having a periphery, said at least one contact pad having at least a portion thereof extending at least partially over said layer comprising substantially diamond adjacent said at least one aperture therein and having at least a portion thereof extending through said at least one aperture in said layer comprising substantially diamond connected to at least one circuit on said substrate.
2. (Previously Presented) The assembly according to claim 1, wherein said periphery of said at least one contact pad covers portions of said layer comprising substantially diamond adjacent said at least one aperture therein.
3. (Original) The assembly according to claim 1, further comprising a conductive bump deposited on said at least one contact pad.
4. (Canceled)
5. (Currently Amended) The assembly according to claim [4] 1, wherein at least one of said passivation layer and said second passivation layer has at least one trace having at least a portion thereof located on a portion of at least one of said passivation layer and said second passivation layer to connect said substrate and said at least one contact pad.

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6. (Currently Amended) The assembly according to claim [4] 1, wherein said passivation layer and said second passivation layer [comprises] comprise a polyimide.
7. (Previously Presented) The assembly according to claim 1, wherein said layer comprising substantially diamond has a thickness of at least about 50 angstroms.
8. (Previously Presented) The assembly according to claim 1, wherein said layer comprising substantially diamond has a thickness of between about 50 and 2000 angstroms.
9. (Withdrawn) The assembly according to claim 1, ~~further comprising: wherein~~ said passivation layer comprises a second layer comprising substantially diamond located between said substrate and said layer comprising substantially diamond.
10. (Withdrawn) The assembly according to claim 9, wherein at least one of said layer comprising substantially diamond and said second layer comprising substantially diamond has at least a portion of one trace located on a portion thereof to connect said substrate and said at least one contact pad.
11. (Withdrawn) The assembly according to claim 9, ~~further comprising: wherein~~ said a second passivation layer includes a layer located between said layer comprising substantially diamond and said second layer comprising substantially diamond.
12. (Withdrawn) The assembly according to claim 11, wherein said second passivation layer has at least a portion of at least one trace located thereon to connect said substrate and said at least one contact pad.
13. (Withdrawn) The assembly according to claim 5, further comprising:  
a film comprising diamond formed between said passivation layer and said substrate, said film directly contacting said surface of said substrate.

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14. (Original) The assembly according to claim 1, wherein said layer comprising substantially diamond comprises substantially polycrystalline diamond.
15. (Original) The assembly according to claim 1, wherein said layer comprising substantially diamond comprises substantially amorphous diamond.
16. (Original) The assembly according to claim 1, wherein said layer comprising substantially diamond comprises polycrystalline diamond and amorphous diamond.
17. (Previously Presented) The assembly according to claim 1, wherein said layer comprising substantially diamond includes one of polycrystalline diamond, amorphous diamond and another material.
18. (Previously Presented) The assembly according to claim 1, wherein said layer comprising substantially diamond includes polycrystalline diamond, amorphous diamond and another material.
19. (Original) The assembly according to claim 1, wherein said substrate comprises: a semiconductor die.
20. (Original) The assembly according to claim 1, wherein said substrate comprises: a bare semiconductor die.
21. (Original) The assembly according to claim 1, wherein said substrate comprises: a semiconductor wafer.
22. (Original) The assembly according to claim 1, wherein said substrate comprises: a portion of a semiconductor wafer.

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23. (Original) The assembly according to claim 1, wherein said substrate comprises:  
a carrier substrate.

24. (Original) The assembly according to claim 1, wherein said substrate comprises:  
a carrier substrate for a flip-chip semiconductor device assembly.

25. (Original) The assembly according to claim 1, wherein said substrate comprises:  
a carrier substrate having a semiconductor die attached thereto.

26. (Original) The assembly according to claim 1, wherein said substrate comprises:  
a carrier substrate having a semiconductor die adhesively attached thereto.

27. (Currently Amended) A semiconductor die assembly comprising:  
a substrate having a surface, a passivation layer, said passivation layer provided over at least a portion of said surface of said substrate, a second passivation layer, said second passivation layer provided over said passivation layer, a layer including diamond having at least one aperture therein, said layer provided substantially over said surface of said substrate, second passivation layer, and at least one contact pad having at least a portion thereof extending at least partially over said layer and having a portion thereof extending at least into said at least one aperture in said layer.

28. (Original) The assembly according to claim 27, wherein said at least one contact pad has substantially a periphery thereof contacting said layer.

29. (Original) The assembly according to claim 27, further comprising:  
a conductive bump located on said at least one contact pad.

30. (Canceled)

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31. (Currently Amended) The assembly according to claim ~~30~~ 27, wherein at least one of said passivation layer and said second passivation layer carries at least one trace to electrically connect said substrate and said at least one contact pad.
32. (Currently Amended) The assembly according to claim ~~30~~ 27, wherein said passivation layer and said second passivation layer [~~comprises~~] comprise a polyimide.
33. (Original) The assembly according to claim 27, wherein said layer has a thickness of at least about 50 angstroms.
34. (Previously Presented) The assembly according to claim 27, wherein said layer has a thickness of between about 50 and 2000 angstroms.
35. (Withdrawn) The assembly according to claim 27, ~~further comprising:~~ wherein said passivation layer comprises a second layer including diamond located between said substrate and said layer.
36. (Withdrawn) The assembly according to claim 35, wherein at least one of said layer and said second layer has at least one trace connecting said substrate and said at least one contact pad.
37. (Withdrawn) The assembly according to claim 35, ~~further comprising:~~ wherein said a second passivation layer includes a layer between said layer and said second layer.
38. (Withdrawn) The assembly according to claim 37, wherein said second passivation layer has at least one trace connecting said substrate and said at least one contact pad.

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39. (Withdrawn) The assembly according to claim 31, further comprising:  
a film including diamond formed between said passivation layer and said substrate, said film contacting said surface of said substrate.
40. (Currently Amended) A heat sink disposed on a substrate comprising:  
a passivation layer disposed on at least a portion of a surface of a substrate;  
a second passivation layer disposed on at least a portion of said passivation layer;  
a layer including diamond disposed on at least a portion of ~~a surface of a substrate~~ said second  
passivation layer, said layer including at least one opening therein; and  
at least one pad located on at least a portion of said surface of said substrate, said at least one pad  
having a portion thereof extending over at least a portion of said layer and having a  
portion thereof located in said at least one opening.
41. (Previously Presented) The heat sink according to claim 40, wherein said at least one pad has more than one portion thereof extending over said at least said portion of said layer.
42. (Canceled)
43. (Currently Amended) The heat sink according to claim ~~[42]~~ 40, wherein at least one of said passivation layer and said second passivation layer has at least one trace connecting said substrate and said at least one pad.
44. (Withdrawn) The heat sink according to claim 40, ~~further comprising; wherein~~  
said passivation layer comprises a second layer including diamond located between said substrate and said layer.
45. (Withdrawn) The heat sink according to claim 44, wherein at least one of said layer and said second layer has at least one trace connecting said substrate and said at least one pad.

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46. (Withdrawn) The heat sink according to claim 44, ~~further comprising: wherein~~  
said a second passivation layer is between said layer and said second layer.

47. (Withdrawn) The heat sink according to claim 46, wherein said second  
passivation layer has at least one trace connecting said substrate and said at least one pad.

48. (Withdrawn) The heat sink according to claim [42] 40, further comprising:  
a film including diamond formed between said passivation layer and said substrate, said film  
contacting said substrate.

49. (Currently Amended) A semiconductor device assembly comprising:  
a semiconductor device having an active surface, having a passivation layer provided over at  
least a portion of said active surface of said semiconductor device, having a second  
passivation layer provided over at least a portion of said passivation layer, having a layer  
comprising substantially diamond provided over at least a portion of said ~~active surface of~~  
~~said semiconductor device~~ second passivation layer having at least one aperture therein,  
and having at least one bond pad having a periphery located on said active surface, said at  
least one bond pad having at least a portion thereof extending at least partially over said  
layer comprising substantially diamond adjacent said at least one aperture therein and  
having at least a portion thereof extending at least through a portion of said at least one  
aperture in said layer comprising substantially diamond, said at least one bond pad  
connected to at least one circuit on said semiconductor device; and  
a substrate.

50. (Previously Presented) The assembly according to claim 49, wherein said  
periphery of said at least one bond pad covers portions of said layer adjacent said at least one  
aperture therein.

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51. (Original) The assembly according to claim 49, further comprising:  
a conductive bump deposited on said at least one bond pad.

52. (Canceled)

53. (Currently Amended) The assembly according to claim ~~52~~ 49, wherein at least one of said passivation layer and said second passivation layer has at least one trace having at least a portion thereof located on a portion of at least one of said passivation layer and said second passivation layer to connect said semiconductor device and said at least one bond pad.

54. (Currently Amended) The assembly according to claim ~~52~~ 49, wherein said passivation layer and said second passivation layer comprise[s] a polyimide.

55. (Original) The assembly according to claim 49, wherein said layer comprising substantially diamond has a thickness of at least about 50 angstroms.

56. (Previously Presented) The assembly according to claim 49, wherein said layer comprising substantially diamond has a thickness of between about 50 and 2000 angstroms.

57. (Withdrawn) The assembly according to claim 49, ~~further comprising: wherein~~ said passivation layer comprises a second layer comprising substantially diamond located between said semiconductor device and said layer comprising substantially diamond.

58. (Withdrawn) The assembly according to claim 57, wherein at least one of said layer comprising substantially diamond and said second layer comprising substantially diamond has at least a portion of one trace located on a portion thereof to connect said substrate and said at least one bond pad.



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59. (Withdrawn) The assembly according to claim 57, ~~further comprising: wherein~~ said a second passivation layer is located between said layer comprising substantially diamond and said second layer comprising substantially diamond.

60. (Withdrawn) The assembly according to claim 59, wherein said second passivation layer has at least a portion of at least one trace located thereon to connect said substrate and said at least one bond pad.

61. (Withdrawn) The assembly according to claim 53, further comprising:  
a film comprising diamond formed between said passivation layer and said semiconductor device, said film directly contacting said active surface of said semiconductor device.

62. (Original) The assembly according to claim 49, wherein said layer comprising substantially diamond comprises substantially polycrystalline diamond.

63. (Original) The assembly according to claim 49, wherein said layer comprising substantially diamond comprises substantially amorphous diamond.

64. (Original) The assembly according to claim 49, wherein said layer comprising substantially diamond comprises polycrystalline diamond and amorphous diamond.

65. (Original) The assembly according to claim 49, wherein said layer comprising substantially diamond includes one of polycrystalline diamond, amorphous diamond, and another material.

66. (Previously Presented) The assembly according to claim 49, wherein said layer comprising substantially diamond includes polycrystalline diamond, amorphous diamond and another material.

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67. (Original) The assembly according to claim 49, wherein said semiconductor device comprises:  
a semiconductor die.

68. (Original) The assembly according to claim 49, wherein said semiconductor device comprises:  
a bare semiconductor die.

69. (Original) The assembly according to claim 49, wherein said semiconductor device comprises:  
a semiconductor wafer.

70. (Original) The assembly according to claim 49, wherein said semiconductor device comprises:  
a portion of a semiconductor wafer.

71. (Original) The assembly according to claim 49, wherein said semiconductor device comprises:  
a flip-chip semiconductor die.

72. (Original) The assembly according to claim 49, wherein said substrate comprises:  
a carrier substrate for a flip-chip semiconductor device assembly.

73. (Original) The assembly according to claim 49, wherein said substrate comprises:  
a carrier substrate having a semiconductor die attached thereto.

74. (Original) The assembly according to claim 67, wherein said substrate comprises:  
a carrier substrate having said semiconductor die adhesively attached thereto.

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75. (Currently Amended) A semiconductor die assembly comprising:  
a semiconductor die having an active surface, a passivation layer, said passivation layer provided substantially over a portion of said active surface of said semiconductor device, a second passivation layer, said second passivation layer provided substantially over a portion of said passivation layer, a layer having at least one aperture therein, said layer including diamond provided substantially over a portion of said active surface of said semiconductor die second passivation layer, and at least one bond pad having at least a portion thereof extending at least partially over said layer and having a portion thereof extending at least into said at least one aperture in said layer; and  
a substrate having said semiconductor die attached thereto.

76. (Original) The assembly according to claim 75, wherein said at least one bond pad has substantially a periphery thereof contacting said layer.

77. (Original) The assembly according to claim 75, further comprising:  
a conductive bump located on said at least one bond pad.

78. (Canceled)

79. (Currently Amended) The assembly according to claim ~~78~~ 75, wherein at least one of said passivation layer and said second passivation layer has at least one trace connecting said semiconductor die and said at least one bond pad.

80. (Currently Amended) The assembly according to claim ~~78~~ 75, wherein said passivation layer and said second passivation layer comprise[s] a polyimide.

81. (Original) The assembly according to claim 75, wherein said layer has a thickness of at least about 50 angstroms.

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82. (Previously Presented) The assembly according to claim 75, wherein said layer has a thickness of between about 50 and 2000 angstroms.

83. (Withdrawn) The assembly according to claim 75, ~~further comprising: wherein~~ said passivation layer comprises a second layer including diamond located between said semiconductor die and said layer.

84. (Withdrawn) The assembly according to claim 83, wherein at least one of said layer and said second layer has at least one trace connecting said semiconductor die and said at least one bond pad.

85. (Withdrawn) The assembly according to claim 84, ~~further comprising: wherein~~ said a second passivation layer is between said layer and said second layer.

86. (Withdrawn) The assembly according to claim 85, wherein said second passivation layer has at least one trace connecting said semiconductor die and said at least one bond pad.

87. (Withdrawn) The assembly according to claim ~~78~~ 75, further comprising:  
a film including diamond formed between said passivation layer and said semiconductor die, said film contacting said active surface of said semiconductor die.

88. (Currently Amended) A heat sink disposed on a semiconductor device comprising:  
a passivation layer disposed on at least a portion of an active surface of a semiconductor device,  
a second passivation layer disposed on at least a portion of said passivation layer,  
a layer including diamond disposed on at least a portion of ~~an active surface of a semiconductor device~~  
said second passivation layer, said layer including at least one opening therein; and

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at least one bond pad located on at least a portion of said active surface of said semiconductor device, said at least one bond pad having a portion thereof extending over at least a portion of said layer and having another portion thereof located in said at least one opening.

89. (Previously Presented) The heat sink according to claim 88, wherein said at least one bond pad has more than one portion thereof extending over said at least a portion of said layer.

90. (Canceled)

91. (Currently Amended) The heat sink according to claim ~~90~~ 88, wherein at least one of said passivation layer and said second passivation layer has at least one trace connecting said semiconductor device and said at least one bond pad.

92. (Withdrawn) The heat sink according to claim 88, ~~further comprising: wherein~~ said passivation layer comprises a second layer including diamond located between said semiconductor device and said layer.

93. (Withdrawn) The heat sink according to claim 92, wherein at least one of said layer and said second layer has at least one trace connecting said semiconductor device and said at least one bond pad.

94. (Withdrawn) The heat sink according to claim 92, ~~further comprising: wherein~~ said a second passivation layer is between said layer and said second layer.

95. (Withdrawn) The heat sink according to claim 94, wherein said second passivation layer has at least one trace connecting said semiconductor device and said at least one bond pad.

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96. (Withdrawn) The heat sink according to claim ~~90~~ 88, further comprising:  
a film including diamond formed between said passivation layer and said semiconductor device,  
said film contacting said semiconductor device.

97. (Currently Amended) A semiconductor die comprising:  
a substrate having a surface, at least one circuit located on said substrate, a passivation layer  
provided over at least a portion of said surface of said substrate, a second passivation  
layer provided over at least a portion of said passivation layer, a layer including diamond  
provided over at least a portion of said surface of said substrate, second passivation layer  
having at least one aperture therein, and having at least one contact pad having a  
periphery, said at least one contact pad having at least a portion thereof extending at least  
partially over said layer adjacent said at least one aperture therein and having at least a  
portion thereof extending through said at least one aperture in said layer, said at least one  
contact pad connected to said at least one circuit on said substrate.

98. (Previously Presented) The semiconductor die according to claim 97, wherein  
said periphery of said at least one contact pad covers portions of said layer adjacent said at least  
one aperture therein.

99. (Original) The semiconductor die according to claim 97, further comprising:  
a conductive bump deposited on said at least one contact pad.

100. (Canceled)

101. (Currently Amended) The semiconductor die according to claim ~~100~~ 97, wherein  
at least one of said passivation layer and said second passivation layer has at least one trace  
having at least a portion thereof located on a portion of at least one of said passivation layer and  
said second passivation layer to connect said substrate and said at least one contact pad.

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102. (Currently Amended) The semiconductor die according to claim ~~100~~ 97, wherein said passivation layer and said second passivation layer comprise[s] a polyimide.

103. (Original) The semiconductor die according to claim 97, wherein said layer has a thickness of at least about 50 angstroms.

104. (Original) The semiconductor die according to claim 97, wherein said layer has a thickness of between about 50 and 2000 angstroms.

105. (Withdrawn) The semiconductor die according to claim 97, ~~further comprising:~~ wherein said passivation layer comprises a second layer including diamond located between said substrate and said layer.

106. (Withdrawn) The semiconductor die according to claim 105, wherein at least one of said layer and said second layer has at least a portion of one trace located on a portion thereof to connect said substrate and said at least one contact pad.

107. (Withdrawn) The semiconductor die according to claim 105, ~~further comprising:~~ wherein said a second passivation layer is located between said layer and said second layer.

108. (Withdrawn) The semiconductor die according to claim 107, wherein said second passivation layer has at least a portion of at least one trace located thereon to connect said substrate and said at least one contact pad.

109. (Withdrawn) The semiconductor die according to claim 101, further comprising: a film including diamond formed between said passivation layer and said substrate, said film directly contacting said surface of said substrate.

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110. (Original) The semiconductor die according to claim 97, wherein said layer comprises substantially polycrystalline diamond.

111. (Original) The semiconductor die according to claim 97, wherein said layer comprises substantially amorphous diamond.

112. (Original) The semiconductor die according to claim 97, wherein said layer comprises polycrystalline diamond and amorphous diamond.

113. (Previously Presented) The semiconductor die according to claim 97, wherein said layer includes one of polycrystalline diamond, amorphous diamond and another material.

114. (Previously Presented) The semiconductor die according to claim 97, wherein said layer includes polycrystalline diamond, amorphous diamond and another material.

115. (Original) The semiconductor die according to claim 97, wherein said substrate comprises:  
a semiconductor wafer.

116. (Original) The semiconductor die according to claim 97, wherein said substrate comprises:  
a portion of a semiconductor wafer.

117. (Withdrawn) A computer assembly comprising:  
at least one input device;  
at least one output device;  
at least one microprocessor connected to said at least one input device and said at least one output device; and



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a substrate connected to said at least one microprocessor, said substrate having a surface, at least one circuit located on said substrate, a layer including diamond provided over at least a portion of said surface of said substrate having at least one aperture therein, and having at least one contact pad having a periphery, said at least one contact pad having at least a portion thereof extending at least partially over said layer adjacent said at least one aperture therein and having at least a portion thereof extending through said at least one aperture in said layer connected to said at least one circuit on said substrate.

118. (Withdrawn) The computer assembly according to claim 117, wherein said periphery of said at least one contact pad covers portions of said layer adjacent said at least one aperture therein.

119. (Withdrawn) The computer assembly according to claim 117, further comprising: a conductive bump deposited on said at least one contact pad.

120. (Withdrawn) The computer assembly according to claim 117, further comprising: a passivation layer located between said substrate and said layer.

121. (Withdrawn) The computer assembly according to claim 120, wherein said passivation layer has at least one trace having at least a portion thereof located on a portion of said passivation layer to connect said substrate and said at least one contact pad.

122. (Withdrawn) The computer assembly according to claim 120, wherein said passivation layer comprises a polyimide.

123. (Withdrawn) The computer assembly according to claim 117, wherein said layer has a thickness of at least about 50 angstroms.

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124. (Withdrawn) The computer assembly according to claim 117, wherein said layer has a thickness of between about 50 and 2000 angstroms.

125. (Withdrawn) The computer assembly according to claim 117, further comprising: a second layer including diamond located between said substrate and said layer.

126. (Withdrawn) The computer assembly according to claim 125, wherein at least one of said layer and said second layer has at least a portion of one trace located on a portion thereof to connect said substrate and said at least one contact pad.

127. (Withdrawn) The computer assembly according to claim 125, further comprising: a passivation layer located between said layer and said second layer.

128. (Withdrawn) The computer assembly according to claim 127, wherein said passivation layer has at least a portion of at least one trace located thereon to connect said substrate and said at least one contact pad.

129. (Withdrawn) The computer assembly according to claim 120, further comprising: a film including diamond formed between said passivation layer and said substrate, said film directly contacting said surface of said substrate.

130. (Withdrawn) The computer assembly according to claim 117, wherein said layer comprises substantially polycrystalline diamond.

131. (Withdrawn) The computer assembly according to claim 117, wherein said layer comprises substantially amorphous diamond.

132. (Withdrawn) The computer assembly according to claim 117, wherein said layer comprises polycrystalline diamond and amorphous diamond.

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133. (Withdrawn) The computer assembly according to claim 117, wherein said layer includes one of polycrystalline diamond, amorphous diamond and another material.

134. (Withdrawn) The computer assembly according to claim 117, wherein said layer includes polycrystalline diamond, amorphous diamond and another material.

135. (Withdrawn) The computer assembly according to claim 117, wherein said substrate comprises:  
a semiconductor wafer.

136. (Withdrawn) The computer assembly according to claim 117, wherein said substrate comprises:  
a portion of a semiconductor wafer.